REMARKS

Claims 1-13 are presented for examination. Claims 1, 4, 7, 10 and 13 are allowed.

REJECTION UNDER 35 U.S.C. § 102

Claims 2-3 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Sourgen. The Examiner's rejection is respectfully traversed for the following reasons.

It is well settled that the Examiner bears the initial burden of establishing a ***prima facie*** basis to deny patentability to a claimed invention under any statutory provision. ***In re Oetiker***, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). Anticipation under 35 U.S.C. § 102 requires the disclosure in a single reference of each element of a claimed invention. ***Minnesota Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.***, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 102, it is incumbent upon the Examiner to point out specifically wherein an applied reference discloses each feature of the claimed invention. ***In re Rijckaert***, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); ***Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.***, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984). It is respectfully submitted that the Examiner did not discharge that burden.

Claim 2 recites a data storage apparatus comprising a scrambling circuit for converting an input signal to a desired format, and a storage device for storing converted data. The claim requires the scrambling circuit to be constituted by a rewritable device.

The Examiner did not point out specifically wherein the reference discloses that the scrambling device is constituted by a rewritable device. The Examiner relies upon claim 2 of Sourgen for disclosing the claimed feature.

However, claim 2 of the patent does not describe that the scrambling circuit is constituted by a rewritable device. Instead, claim 2 recites that the central interconnecting layer and the local

interconnecting layer are ion implanted silicon.

In the event the Examiner relied upon inherency without expressly indicating such reliance, the Examiner should be aware that inherency requires certainty, not speculation. ***In re Rijckaert***, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); ***In re King***, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); ***W. L. Gore & Associates, Inc. v. Garlock, Inc.***, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); ***In re Oelrich***, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); ***In re Wilding***, 535 F.2d 631, 190 USPQ 59 (CCPA 1976). To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

However, the Examiner provided no factual basis upon which to conclude that the ion implanted silicon is necessarily a rewritable device.

Moreover, Sourgen discloses scrambling by permutation of data bits using permutation circuits DBr2 and DBr3. However, the reference provides no reason to conclude that the permutation circuits are constituted by a rewritable device.

The reference discloses that data supplied from the permutation circuits may be stored by rewritable memories. However, the data are supplied to the rewritable memories in a scrambled form (col. 3, lines 55-57). Therefore, the rewritable memories are not part of a scrambling circuit.

Therefore, the reference does not disclose that the scrambling circuit is constituted by a rewritable device, as claim 2 requires.

Further, claim 3, dependent from claim 2, recites that the scrambling circuit includes:

- a plurality of conversion circuits each converting said input signal according to different rules; and

- a selector for selecting one of signals output by said plurality of conversion circuits and supplying what is selected to said storage device.

The Examiner takes the position that the reference inherently discloses the claimed selector based on the Sourgen's teaching of "selection of the bits permutation different from a rewritable memory to another (sic)" (col. 4, lines 6-7).

However, the reference discloses that the data from the permutation circuit DBr2 are supplied only to the RAM, and the data from the permutation circuit DBr3 are supplied only to the EEPROM. No selector is provided for selecting one of signals output from these permutation circuits, and supplying what is selected to the storage device, as claim 3 recites. Accordingly, Sourgen does not disclose the claimed selector.

Moreover, one skilled in the art would understand that Sourgen teaches away from a selector for selecting one of the outputs of the permutation circuit, because the reference indicates that "data are differently scrambled according to the memory where it is memorized" (col. 4, lines 10-11). Hence, the data scrambled by the permutation circuit DBr2 must be transferred only to the RAM, whereas the data scrambled by the permutation circuit DBr3 must be directed only to the EEPROM. Therefore, the selector at the outputs of the permutation circuits is not needed.

Accordingly, Sourgen et al. does not describe the invention recited in claims 2 and 3 within the meaning of 35 U.S.C. § 102. ***Minnesota Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., supra.*** Applicants, therefore, respectfully submit that the rejection of claims 2 and 3 under 35 U.S.C. § 102 as anticipated by Sourgen et al. is untenable and should be withdrawn.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 5-6 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Sourgen et al. in view of Kato et al. Claims 8-9 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Sourgen et al. in view of Maeda. Claims 11-12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Sourgen et al. in view of Itoi.

Claims 5, 6, 8, 9, 11 and 12 depend from claim 2 or 3. Therefore, they are defined over Sourgen et al. at least for the reasons presented above in connection with claims 2 and 3.

Further, in the application of a rejection under 35 U.S.C. §103, it is incumbent upon the Examiner to factually support a conclusion of obviousness. The Examiner must provide reasons why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. ***Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.***, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985). ***In re Fine***, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); ***Stratoflex, Inc. v. Aeroquip Corp.***, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); ***In re Warner***, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). These showings by the Examiner are an essential part of complying with the burden of presenting a *prima facie* case of obviousness. ***In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

However, the Examiner has failed to provide the requisite reasons for modifying Sourgen et al., and thus to establish a *prima facie* case of obviousness.

For example, the Examiner suggests modifying Sourgen to include address generator for generating address signals for storage location in response to external commands as taught by Maeda. The Examiner believes that such a modification "would simplify the specification of address and complicated control become needless."

However, the object of the Sourgen's invention is to improve protection of data in a program memory. The data are protected by mixing memory address data and instructions stored at that memory address. The reference teaches that the data are not arranged in the memory according to logical address, but are scattered around the memory (col. 1, lines 13-17).

Accordingly, the modification suggested by the Examiner would result in deterioration of the data protection in the Sourgen's system. However, it is well settled that if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. ***In re Gordon***, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

Further, one skilled in the art would understand that there is no motivation to add the A/D converter of Kato into the Sourgen system because Sourgen does not use analog signals.

Moreover, one skilled in the art would find no reason to include the compression circuit of Itoi into the Sourgen's system, as the Examiner suggests. The Sourgen reference discloses mixing scrambled and unscrambled data in order to improve data protection. One skilled in the art would understand that the compression of data suggested by the Examiner would make it more difficult to mix scrambled and unscrambled data. Hence, this modification would render Sourgen's invention being modified unsatisfactory for its intended purpose.

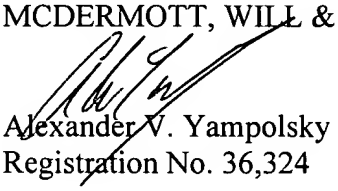
Accordingly, Applicants submit that the lack of any motivation for the proposed combination of references to arrive at the claimed invention undermines the basis for the Examiner's rejections under 35 U.S.C. § 103. Applicants, therefore, respectfully submit that the rejections of claims 5, 6, 8, 9, 11 and 12 under 35 U.S.C. § 103 are improper and should be withdrawn.

In view of the foregoing, and in summary, claims 1-13 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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